

FIG. 1  
(PRIOR ART)

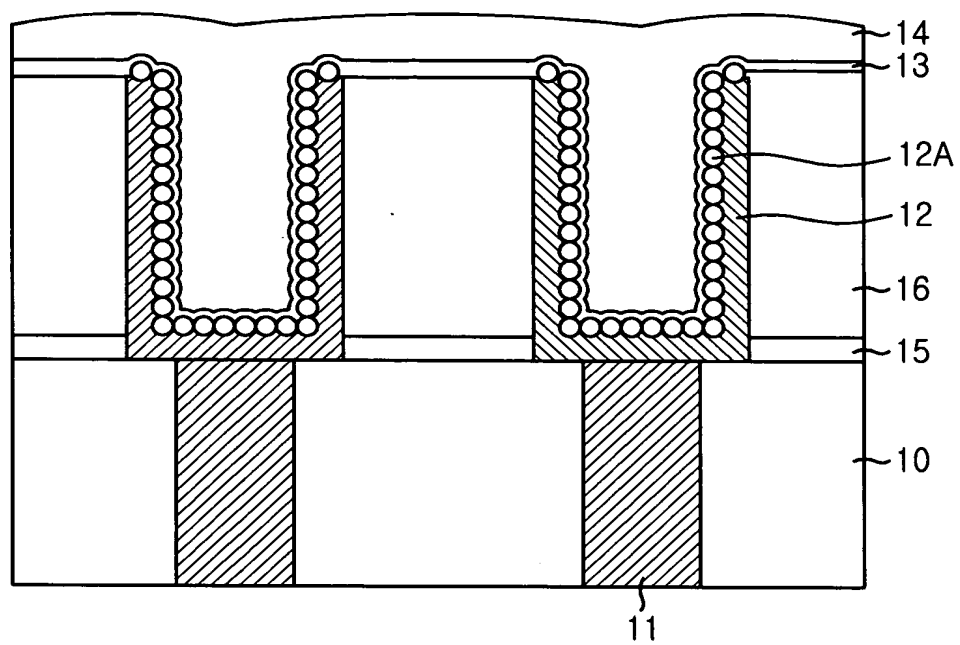
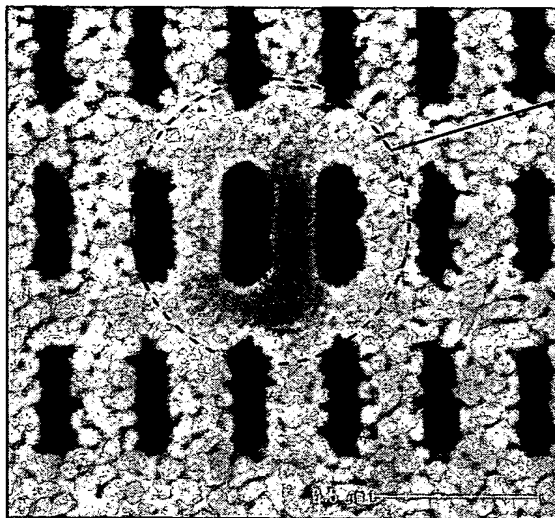


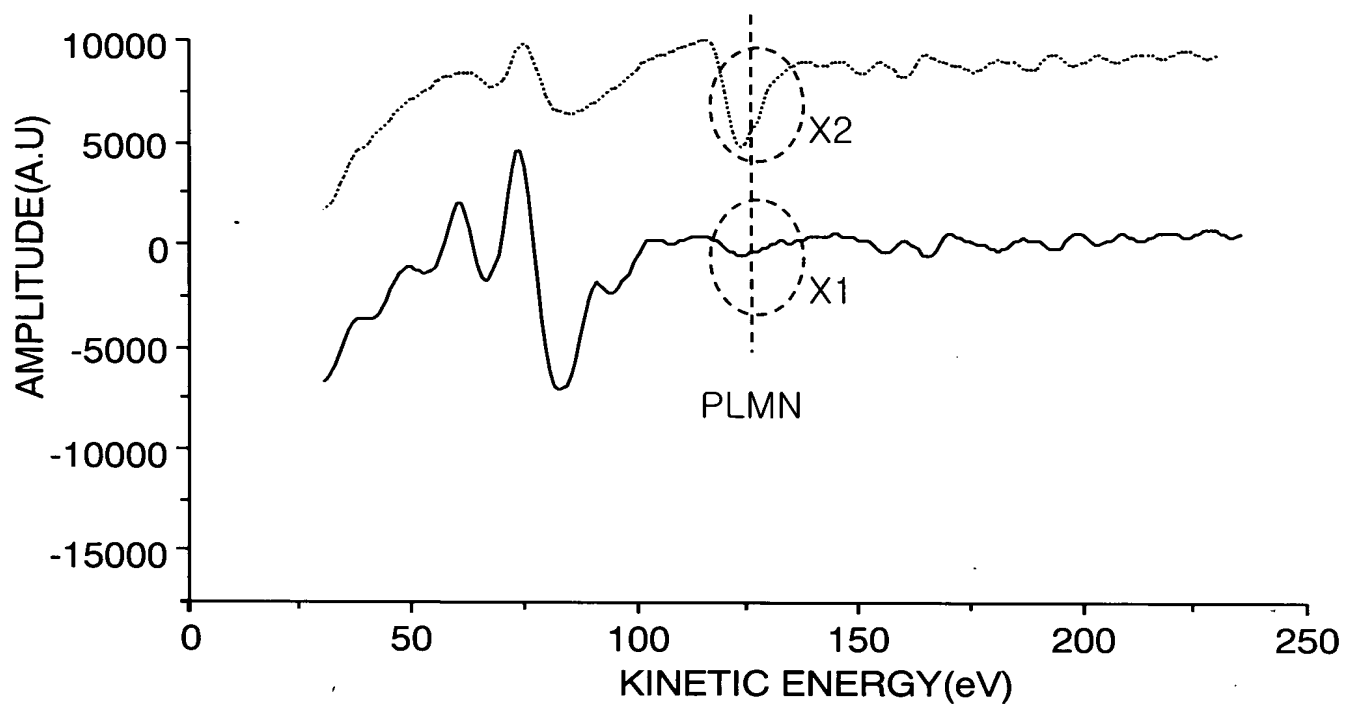
FIG. 2A  
(PRIOR ART)



MPS GROWTH  
SUPPRESSION  
REGION

BEST AVAILABLE COPY

FIG. 2B  
(PRIOR ART)



A schematic diagram of a multi-layered structure. It consists of a base layer (21) and a top layer (24). The base layer (21) is divided into five rectangular regions. The second and fourth regions from the left are filled with diagonal hatching. The top layer (24) is divided into three rectangular regions, each positioned above one of the unhatched regions of the base layer. A label 22 points to the boundary between the first and second regions of the base layer. A label 23 points to the boundary between the second and third regions of the base layer.

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 21, a patterned layer 22, a gate stack 23, a channel layer 24, a source/drain region 25, and a contact layer 26.

FIG. 3C

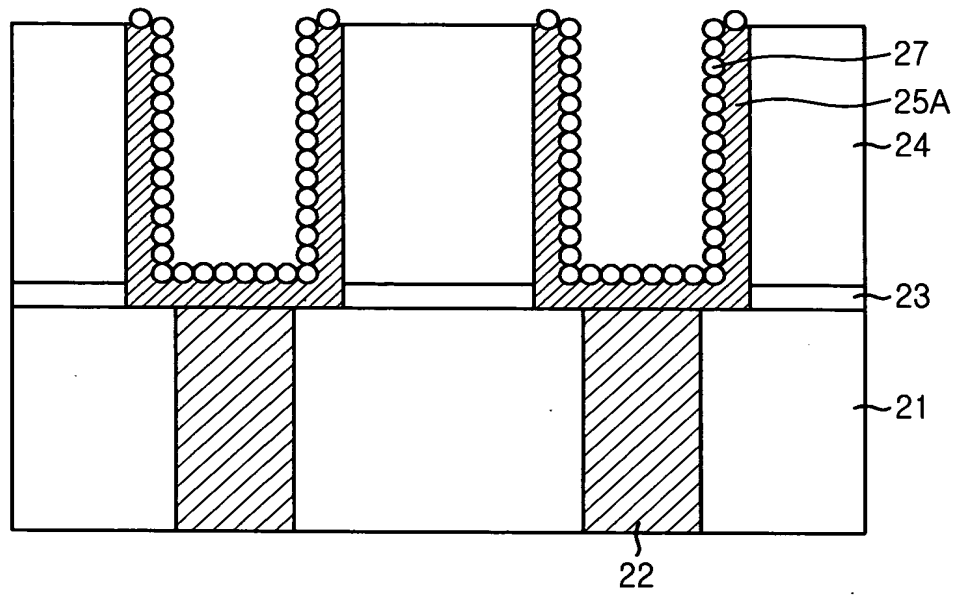


FIG. 3D

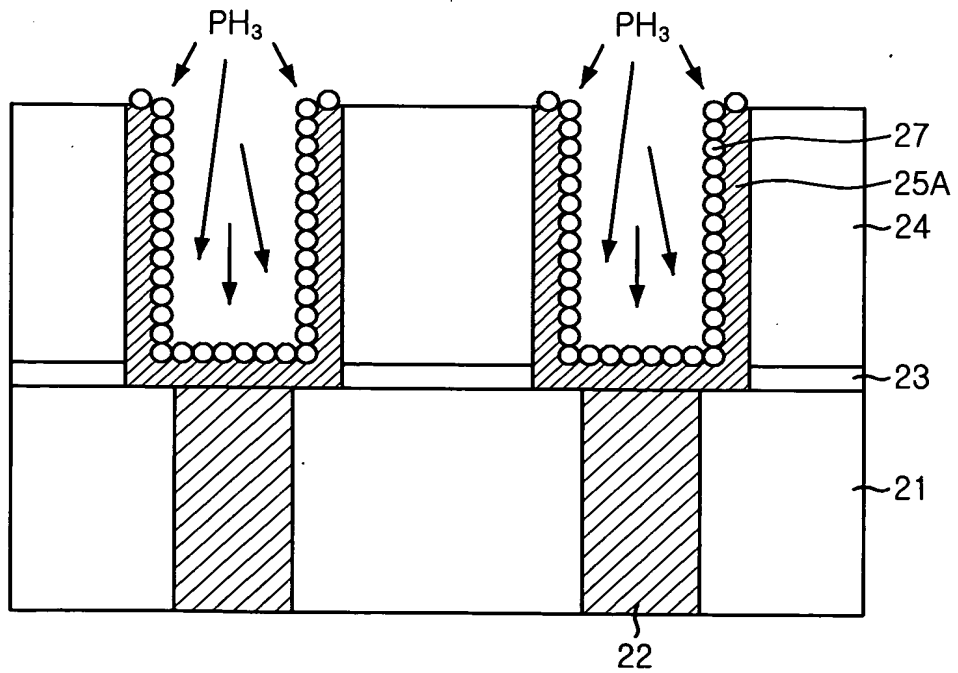


FIG. 3E

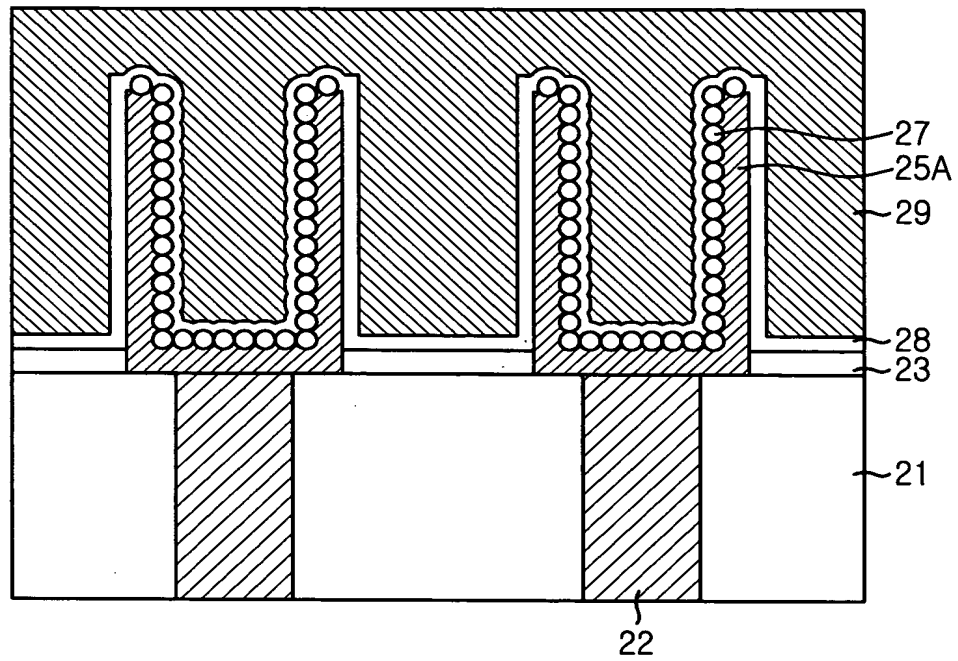


FIG. 4

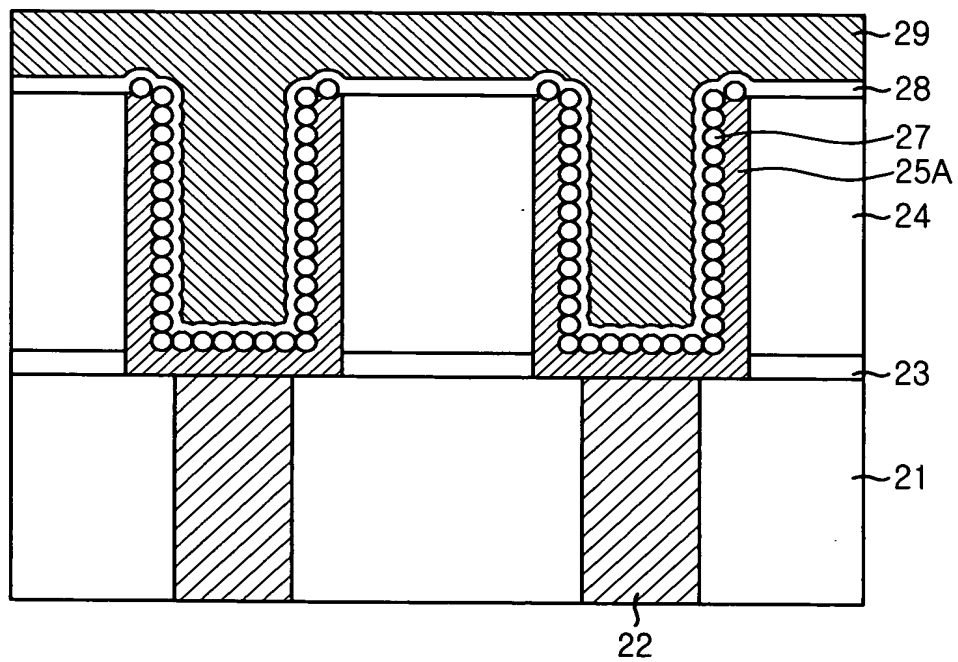


FIG. 5A

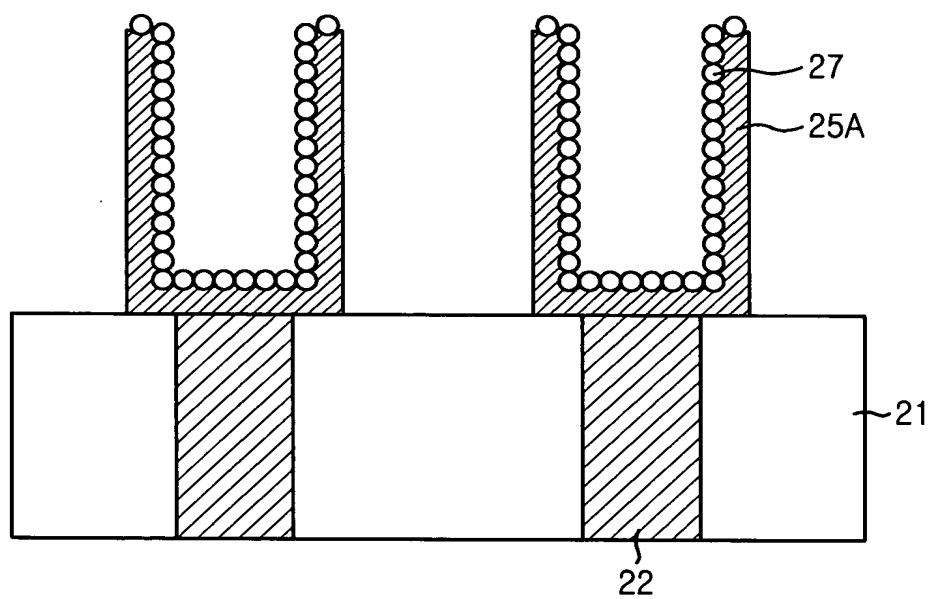


FIG. 5B

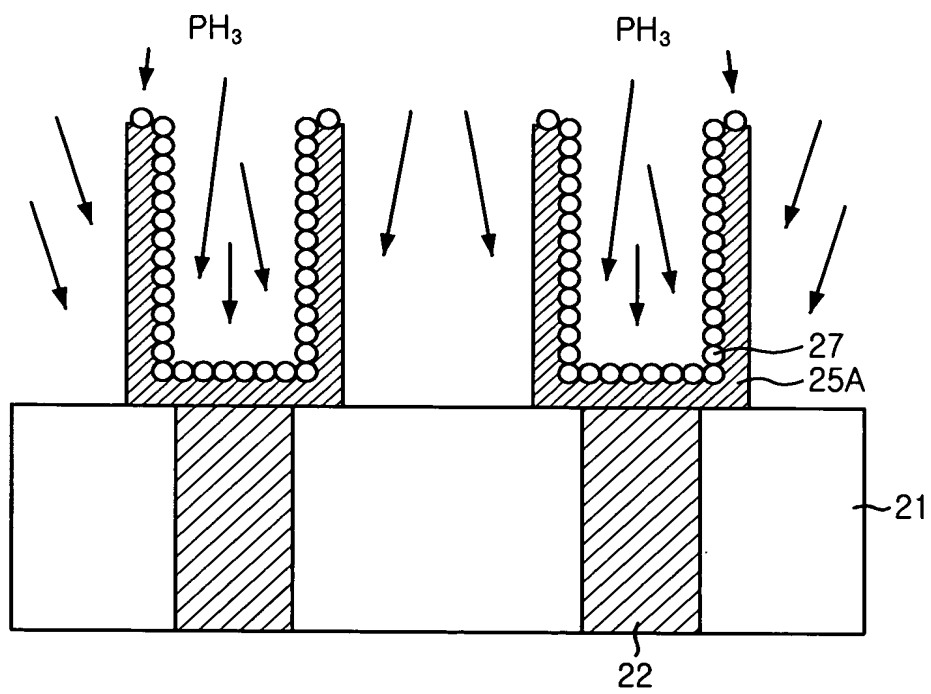


FIG. 5C

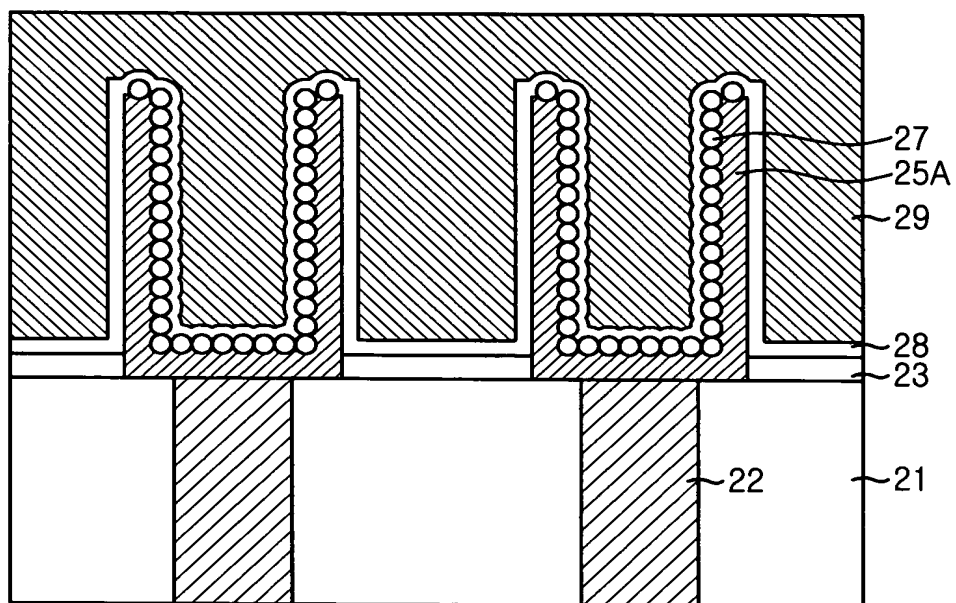


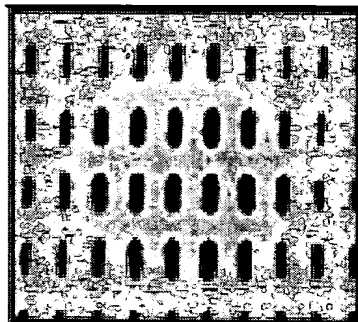


FIG. 6A



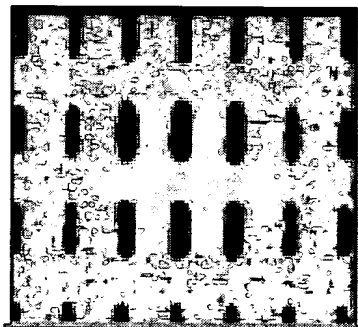
72 POINTS

FIG. 6B



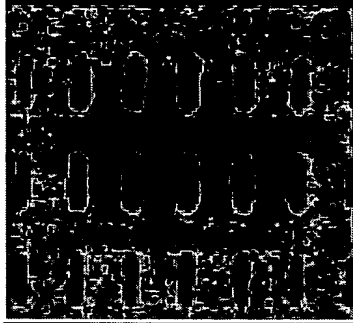
106 POINTS

FIG. 6C



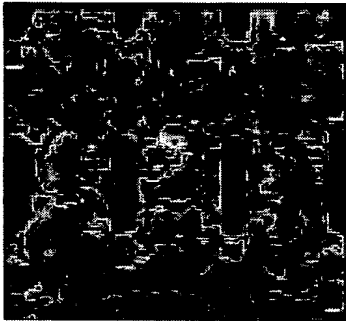
42 POINTS

FIG. 6D



71 POINTS

FIG. 6E



13 POINTS